CLAIMS

What is claimed is:

1. A method comprising:

detecting a plurality of subchannels comprising symbol-modulated orthogonal subcarriers to generate a channelization vector indicating which of the subchannels are active and which of the subchannels are inactive; and

performing data-symbol processing on the active subchannels in response to the channelization vector to generate a bit stream from combined contributions of the active subchannels.

2. The method of claim 1 further comprising generating a decoded bit stream from combined contributions of the active subchannels.

3. The method of claim 1 wherein detecting comprises independently detecting the subchannels of the plurality with a parallel set of matched filters.

4. The method of claim 1 wherein detecting comprises detecting the subchannels with a parallel set of matched filters, wherein each of the matched filters has a coefficient spectrum matched to a corresponding one of the subchannels.

5. The method of claim 1 further comprising refraining from performing data-symbol processing on the inactive of the subchannels in response to the channelization vector.

6. The method of claim 1 further comprising providing the channelization vector to data-symbol processing circuitry,

wherein the data-symbol processing circuitry is responsive to the channelization vector to perform data-symbol processing on the active subchannels, and

wherein the data-symbol processing circuitry is responsive to the channelization vector to turn-off data-symbol processing on the inactive subchannels.

7. The method of claim 6 wherein the performing data-symbol processing comprises performing a fast-Fourier transform on only the active subchannels to generate a bit stream from combined contributions of the active subchannels.

8. The method of claim 1 further comprising:

providing the channelization vector to combiner circuitry; and

combining, with the combiner circuitry, bit streams from the data-symbol processing of the active subchannels to generate a combined bit stream.

9. The method of claim 8 further comprising refraining from combining a processing output generated from the inactive subchannels.

10. The method of claim 1 further comprising:

generating a channelization vector for a plurality of received packets; and

repeating the detecting and performing the data-symbol processing for the received packets, wherein the received packets comprise symbols modulated on a plurality of orthogonal subcarriers of an orthogonal frequency-division multiplexed signal.

11. The method of claim 1 further comprising receiving a synchronized sequence of short-training symbols on at least two of the active subchannels, the sequence of short-training symbols comprising at least a portion of preamble of a received packet,

wherein the detecting comprises sampling the sequence of short-training symbols on the at least two active subchannels, and

wherein the data-symbol processing comprises data-symbol processing a sequence of long-training symbols and data symbols on the active subchannels, the long-training symbols and data symbols following the sequence of short-training symbols in the packet.

12. The method of claim 1 further comprising receiving synchronized data streams on the active subchannels, the synchronized data streams being preceded by a preamble, the channelization vector being generated from detection of the preamble.

13. The method of claim 1 further comprising:

determining channel conditions of the subchannels, the channel conditions including at least one of an interference level and fading; and

sending a request to a transmitter to refrain from transmitting on a subchannel that has poor channel conditions.

14. An apparatus comprising:

short-training symbol processing circuitry to detect a training sequence modulated on a plurality of subchannels and generate a channelization vector indicating which of the subchannels are active and which of the subchannels are inactive; and

data-symbol processing circuitry to process data symbols on the active subchannels in response to the channelization vector.

15. The apparatus of claim 14 wherein the data-symbol processing circuitry refrains from processing the inactive subchannels in response to the channelization vector.

16. The apparatus of claim 14 wherein the short-training symbol processing circuitry comprises a plurality of matched filters, each matched filter having a coefficient spectrum matched to a corresponding one of the subchannels.

17. The apparatus of claim 16 wherein the short-training symbol processing circuitry further comprises:

non-coherent summators to sum output from a corresponding one of the matched filters;

threshold detectors to determine when the summed output from a corresponding one of the summators exceeds a predetermined threshold; and

a multiplexer to combine outputs from the threshold detectors to generate the channelization vector.

18. The apparatus of claim 14 wherein the data-symbol processing circuitry comprises a combiner to generate a combined bit stream from individual bit streams generated by data-symbol processing the active subchannels in response to channelization vector, the combiner to refrain from combining contributions from the inactive subchannels in response to the channelization vector.

19. The apparatus of claim 14 wherein the data-symbol processing circuitry comprises fast-Fourier transform (FFT) circuitry for a predetermined number of the subchannels, channel equalization circuitry, demapping circuitry and deinterleaving circuitry to perform data-symbol processing in parallel for the predetermined number of the subchannels.

20. The apparatus of claim 19 wherein the data-symbol processing circuitry further comprises:

a combiner to a combiner to generate a combined bit stream from individual bit streams generated by data-symbol processing the active subchannels in response to channelization vector; and

a decoder to decode the combined bit stream and generate a decoded bit stream output.

21. The apparatus of claim 19 wherein the data-symbol processing circuitry comprises four 64-bit fast-Fourier transform (FFT) processing circuits to process four 20 MHz subchannels substantially in parallel.

22. The apparatus of claim 14 wherein the data-symbol processing circuitry comprises wideband fast-Fourier transform (FFT) circuitry to selectively perform an FFT on parallel groups of time-domain samples from the

active subchannels in response to the channelization vector and to selectively refrain from performing the FFT on the parallel groups of time-domain samples from the inactive subchannels in further response to the channelization vector.

23. The apparatus of claim 22 wherein the wideband fast-Fourier transform (FFT) circuitry comprises a 256-bit FFT processing circuit to process 256 parallel symbols from a wideband channel comprised of up to four 20 MHz subchannels.

24. The apparatus of claim 19 further comprising a wideband decoder to generate a decoded bit stream from combined bit streams from the active subchannels.

25. A receiver system comprising:

an omnidirectional antenna to receive symbol-modulated subcarriers over a plurality of subchannels;

short-training symbol processing circuitry to detect the plurality of subchannels and generate a channelization vector indicating which of the subchannels are active and which of the subchannels are inactive; and

data-symbol processing circuitry to process data symbols on the active subchannels in response to the channelization vector.

26. The system of claim 25 wherein the short-training symbol processing circuitry comprises:

a plurality of matched filters, each matched filter having a coefficient spectrum matched to a corresponding one of the subchannels;

non-coherent summators to sum output from a corresponding one of the matched filters;

threshold detectors to determine when the summed output from a corresponding one of the summators exceeds a predetermined threshold; and

a multiplexer to combine outputs from the threshold detectors to generate the channelization vector.

27. The system of claim 25 wherein the data-symbol processing circuitry comprises fast-Fourier transform (FFT) circuitry for a predetermined number of the subchannels, channel equalization circuitry, demapping circuitry and deinterleaving circuitry to perform data-symbol processing in parallel for the predetermined number of the subchannels.

28. A machine-readable medium that provides instructions, which when executed by one or more processors, cause said processors to perform operations comprising:

detecting a plurality of subchannels to generate a channelization vector indicating which of the subchannels are active and which of the subchannels are inactive; and

performing data-symbol processing on the active of the subchannels in response to the channelization vector.

29. The machine-readable medium of claim 28 wherein the instructions, when further executed by one or more of said processors, cause said processors to perform operations further comprise generating a decoded bit stream from combined contributions of the active subchannels, and

wherein detecting comprises detecting the subchannels with instructions that implement a parallel set of matched filters, wherein each of the matched filters has a coefficient spectrum matched to a corresponding one of the subchannels.

30. The machine-readable medium of claim 28 wherein the instructions, when further executed by one or more of said processors, cause said processors to perform operations further comprising performing a fast-Fourier transform to generate a bit stream from combined contributions of the active subchannels.